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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/721,970

11/24/2003

Dae Woo Lee

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08/25/2004

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EXAMINER

MALSAWMA, LALRINFAMKIM HMAR


ART UNIT

PAPER NUMBER

2825

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/721,970	<b>Applicant(s)</b> LEE ET AL.	
	<b>Examiner</b> Lex Malsawma	<b>Art Unit</b> 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 24 November 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-4 is/are allowed.
- 6) ☒ Claim(s) 6-13 is/are rejected.
- 7) ☒ Claim(s) 5 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>20031124</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Objections*

1. Claims 5, 6 and 12 are objected to because of the following informalities:

At claim 6, in step (d), the examiner suggests replacing “the” with “a” before “second oxidation”, since this is the first recitation of a second oxidation film.

At claim 6, in step (f), the examiner suggests replacing “etching” with “removing”, since step “(c)” recites, “removing the nitride film”.

At claims 5 and 12, in line 3 (of each claim), the examiner suggests deleting the phrase, “intended to be”, since “an intention to be equal” does not require “equality”.

At claim 12, in line 3, the examiner suggests inserting “region” after “voltage device”.

At claim 12, in the last line, the examiner suggests replacing “the” with “a” before “source and drain” and inserting “region” after “low voltage device”.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 6-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Houston** (6,424,016 B1) in view of **Gilbert et al.** (5,773,326; hereinafter, “**Gilbert**”) and **Maeda et al.** (6,314,021 B1; hereinafter, “**Maeda**”).

*Regarding claim 6:*

Houston discloses a method for manufacturing an array area and a periphery area (Col. 4, lines 14-19) comprising the steps of:

(a) depositing a first oxidation film 34 and a nitride film 35 sequentially on a SOI substrate where a lower substrate 30, a buried oxidation (BOX) film 32, and an upper silicon layer 33 are sequentially stacked (Fig. 2);

(d) growing a second oxidation film 36 in the array area (Fig. 3):

(e) removing the second oxidation film 36 by etching while remaining some portion of the second oxidation film to have a predetermined thickness (i.e., during the process of removing the second oxidation film, some portion will remain until all of the second oxidation film is removed, as required in the next step “(f)”; and

(f) removing the remaining portion of the first oxidation film 34 and the second oxidation film 36 after removing the nitride 35 (note Figs. 3-4).

Houston **lacks** step “(b)”, step “(c)”, and specifying any particular voltage relationship between devices in the periphery area and devices in the array area. In regards to steps “(b)” and “(c)”, note that Houston does not specify how the structure in Fig. 2 is obtained; accordingly, one of ordinary skill in the art would have utilized any well-known process for acquiring such a structure. Gilbert **teaches** a process for thinning a region of an upper silicon layer of a SOI substrate, similar to that disclosed by Houston, wherein Gilbert specifically discloses depositing a first oxidation film 22 (Fig. 2) and a nitride film 24 (Col. 2, lines 30-34); coating a photoresist film 29 (Fig. 2) on the total structure; and removing the nitride film and the first oxidation film (not covered by the patterned photoresist) prior to forming a second oxidation film 35 (Figs. 3-4,

and note Col. 2, lines 40-65). Maeda is **cited only to show** that “the array area” and “the periphery area”, specified by Houston, could be readily referred to as a high-voltage region and a low-voltage region, respectively (note Maeda, Figs. 30 and 35). In other words, Maeda show that high-voltage devices are formed in “an array area” and low-voltage devices are formed in “a periphery area”. Given Gilbert and Maeda, it would have been obvious to one of ordinary skill in the art to modify Houston by specifying high and low voltage device regions (instead of array and periphery areas) and specifically reciting steps “(b)” and “(c)” because Maeda shows that Houston’s array and periphery areas would generally include high and low voltage devices (respectively) and Gilbert teaches a process for acquiring the structure in Fig. 2 of Houston, i.e., since Houston does not specify how the structure in Fig. 2 is acquire, it would have been obvious to incorporate the process disclosed by Gilbert.

*Regarding claims 7 and 9:*

The cited references **lack** the second oxidation film being 6000-8000 Å in thickness and the upper silicon layer of the array area being in a range of 0.2 to about 0.5 µm in thickness. However, note that Gilbert discloses a “starting” thickness for an upper silicon layer 15 is 3000 Å (Col. 2, lines 21-23) and a second oxidation film 35 of approx. 3600 Å (Col. 3, lines 11-15) is sufficient to produce a desired thickness of approx. 0.05 to 0.15µm (Col. 3, lines 47-50) for the upper silicon layer within the thinned area. It is important to note that the process for forming a second oxidation film, as disclosed by both Houston and Gilbert, is/was generally well-known in the art, often referred to as LOCOS (LOCAl Oxidation of Silicon), and the second oxidation film could be easily formed to have any specified range in thickness depending on design requirements, i.e., depending on a particular “starting” thickness for the upper silicon layer, one

could easily form an oxidation film by LOCOS to consume any desired amount of the upper silicon layer such that the remaining portion of the upper silicon layer is sufficiently thin according to design requirement, e.g., note that Gilbert discloses (in Col. 4, lines 20-23) one example in which LOCOS is used to form an oxidation film (42 or 50) having a thickness of about 7000 Å. Therefore, it would have been obvious to one of ordinary skill in the art to modify Houston (in view of Gilbert and Maeda) by forming the second oxidation film and the upper silicon layer to have thicknesses as currently claimed because a particular thickness for the second oxidation and/or the upper silicon layer would depend directly on a particular design requirement, and any desired thickness for either the second oxidation film or the upper silicon layer could be easily acquired by the process(es) disclosed by the cited references, since the process(es) is(were) well known in the art. In other words, the ranges specified in the current claims are considered to be optimum or workable ranges for some particular design requirement. Note it is has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

*Regarding Claim 8:*

Houston (in view of Maeda) discloses the upper silicon layer of the array area (the high-voltage device region) is made to be thinner than the upper silicon layer of the periphery area (the low-voltage device region) by performing steps (d) and (e) once. It would have been an obvious matter of design choice for one of ordinary skill in the art to modify Houston (in view of Gilbert and Maeda) by specifically repeating steps (d) and (e) to acquire the thinned portion of the upper silicon layer because one of ordinary skill in the art would readily recognize that steps

(d) and (e) could be repeated numerous times if so desired, especially since step (f) removes any/all remaining portion(s) of the second oxidation film. In other words, the number of times steps (d) and (e) are performed (e.g., one time or numerous times) is essentially irrelevant, since the end result is that any/all remaining portion of the second oxidation film must be removed in step (f); therefore, one could obviously choose to repeat steps (d) and (e) numerous times if process time and/or cost were not an issue.

*Regarding claim 10:*

Gilbert discloses the process for forming a second oxidation film 35 comprises thermal oxidation (Col. 3, lines 1-5), wherein the thermal oxidation process could obviously be referred to as a high-pressure oxidation growth process, especially since the term “high pressure” is relative and the claimed invention does not quantify the term or recite any limitations that clarifies what would or would not be considered “high pressure”, e.g.,  $1 \times 10^{-8}$  Torr (high vacuum) would be considered to be “high pressure” relative to  $1 \times 10^{-11}$  Torr (ultra-high vacuum), however,  $1 \times 10^{-8}$  Torr (high vacuum) would also be considered to be “extremely low pressure” relative to atmospheric pressure ( $\sim 760$  Torr). Therefore, this claim is held obvious over the cited references.

*Regarding claims 11 and 13:*

These claims are essentially drawn to a structure acquired by the method of claims 6 and 9. Accordingly, these claims are held obvious over the cited references, since all recited structural limitations are included in the method of claims 6 and 9.

*Regarding claim 12:*

Maeda discloses (in Fig. 30) that a junction depth of impurities of a source and drain region 12 is equal to a thickness of the thinner portion of upper silicon layer; accordingly, the instant claim is held obvious over the cited references.

***Allowable Subject Matter***

4. Claims 1-4 and 5(as suggested by the examiner) are allowable over the references of record.

5. The following is a statement of reasons for the indication of allowable subject matter:

Claims 1-5 are allowable primarily because the references of record, singly or in combination, cannot fairly suggest the following limitations (in combination as recited in claim 1): forming a thinner upper silicon layer for the high-voltage-device region, where the high and low voltage device regions are formed (by etching) after defining a device isolation region; and forming a thin gate insulation film in the low-voltage-device region and a thick gate insulation film in the high-voltage-device region

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The references listed on the attached Form PTO-892 (not cited above) are cited to show methods and devices incorporating an SOI substrate having an upper silicon layer, which has



thick and thin portions; and methods for forming high-voltage devices such as lateral DMOS devices incorporated with low voltage devices, etc.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903. The examiner can normally be reached on Mon-Fri (6AM-2PM EST).

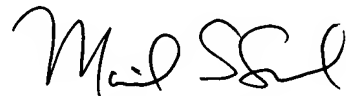
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lex Malsawma



August 12, 2004



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